Add after page 20, line 24 the following paragraph:

a5

The structure shown in Fig. 3 is almost identical with that in Fig. 1, except that the second capacitive element is formed by an interaction of the first supply track 1 and the third supply track 3. The above description in connection with Fig. 1 is also applicable to Fig. 3.

In the Claims:

Cancel claims 2-4.

Claim 1(amended). An integrated circuit, comprising:

a first supply track to be connected to a first supply potential;

a6

a second supply track to be connected to a second supply potential, the first supply potential and the second supply potential supplying a supply voltage, said first supply track and said second supply track forming a first metallic layer;

at least one second metallic layer having at least one third supply track to be connected to one of the first supply potential and the second supply potential and disposed in each case above said first metallic layer;

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at least one first capacitive element disposed below said first metallic layer; and

at least one second capacitive element defined by said at least one third supply track and at least one of said first supply track and said second supply track;

said at least one first capacitive element and said at least one second capacitive element being connected in parallel and smoothing over the supply voltage;

said at least one first capacitive element being one of a plurality of first capacitive elements disposed below both said first supply track and said second supply track, and said at least one second capacitive element being one of a plurality of second capacitive elements;

said second capacitive elements each having a capacitance and said first capacitive elements each having a capacitance being at least a factor of 10 greater than said capacitance of said second capacitive elements.

Claim 2 (amended). The integrated circuit according to claim 1, including:

a substrate having doping regions formed therein; and

a polysilicon layer having at least one poly section disposed above said substrate, said first capacitive elements formed by an interaction of said at least one poly section formed in said polysilicon layer and said doping regions formed in said substrate.

Please Add the Following New Claims:

Claim 8 ~~11~~. An integrated circuit, comprising:

a first supply track to be connected to a first supply potential;

a second supply track to be connected to a second supply potential, the first supply potential and the second supply potential supplying a supply voltage, said first supply track and said second supply track forming a first metallic layer;

at least one second metallic layer having at least one third supply track to be connected to one of the first supply potential and the second supply potential and disposed in each case above said first metallic layer;

a substrate having doping regions formed therein;

a polysilicon layer having at least one poly section disposed above said substrate;

at least one first capacitive element disposed below said first metallic layer, formed by an interaction of said at least one poly section formed in said polysilicon layer and said doping regions formed in said substrate; and

at least one second capacitive element defined by said at least one third supply track and at least one of said first supply track and said second supply track;

said at least one first capacitive element and said at least one second capacitive element being connected in parallel and smoothing over the supply voltage;

said at least one first capacitive element being one of a plurality of first capacitive elements disposed below both said first supply track and said second supply track, and said at least one second capacitive element being one of a plurality of second capacitive elements;

said first capacitive elements and said second capacitive elements each having a capacitive component and a resistive component connected in series with said capacitive component, said resistive component of said second capacitive elements

substantially resulting from conductances of said first metallic layer and said at least one second metallic layer, and said resistive component of said first capacitive elements substantially resulting from conductances of said at least one poly section and of corresponding ones of said doping regions in said substrate;

said resistive component of said first capacitive elements being at least a factor of 10 greater than said resistive component of said second capacitive elements.

8 cont

Claim ~~12~~ 9. The integrated circuit according to claim ~~11~~ 8, wherein said capacitive component of said first capacitive elements is at least a factor of 10 greater than said capacitive component of said second capacitive elements.

Claim ~~13~~ 10. The integrated circuit according to claim ~~11~~ 8, including an insulating material disposed between said at least one poly section and said first and second supply tracks, said insulating material having a plurality of plated-through holes formed therein connecting said first supply track of said first metal layer to said at least one poly section.

Claim ~~14~~ 11. The integrated circuit according to claim ~~11~~ 8, wherein said at least one second capacitive element is formed

by an interaction of said at least one third supply track and said first supply track.

8 cont

Claim ~~15~~ 12. The integrated circuit according to claim ~~11~~ 8, wherein said at least one second capacitive element is formed by an interaction of said at least one third supply track and said second supply track.

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